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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,467	05/07/2004	Che-Li Lin	12919-US-PA	3466

31561 7590 05/12/2009

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
PIZIALI, JEFFREY J	
ART UNIT	PAPER NUMBER
2629	

NOTIFICATION DATE	DELIVERY MODE
05/12/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/709,467	LIN, CHE-LI	
	Examiner	Art Unit	
	Jeff Piziali	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1/22/09, 9/19/08, and 5/14/08*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *5,9,10,15-18 and 20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-8,11-14 and 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 May 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

2. The drawings were received on *14 May 2008*. These drawings are acceptable.

Election/Restrictions

3. ***Applicant's election with traverse of Species I-D-1 (claims 1-4, 6-8, 11-14, and 19)*** in the reply filed on *22 January 2009* is acknowledged.

The traversal is on the ground(s): "*Pertaining to Species I and Species II, the LCD devices respectively disclosed in FIGs. 3 and 5 only differ by the presence of the connector and naming of the similar components, i.e. the ASIC chip 200 compared with the timing sequence control unit 256 and the DC/DC converter 130 compared with the power supply 258. As known to persons having ordinary skills in the art, the connector is a required component of an LCD device, so that whether the connector is explicitly shown or not, it should be appreciated as being present. In addition, by comparing paragraphs [0028], [0032] and [0033] of the specification, it is clear that the ASIC chip 200 and the timing-sequence control unit 256 have very similar functions but different names. The same holds true for the DC/DC converter 130*

and the power supply 258." (see Pages 7-8 of the *22 January 2009* Election). This is not found persuasive.

There is an examination and search burden for argued ***Species I and II*** due to the following mutually exclusive characteristics:

Figure 3 illustrates a connector (*128*) commonly coupled between both a DC/DC converter (*130*) and an ASIC (*200*).

In contrast, Figure 5 illustrates no "connector" whatsoever.

Figure 3 illustrates the DC/DC converter (*130*) coupled to the source drivers (*204*) via two distinct paths.

In contrast, Figure 5 illustrates the power supply (*258*) coupled to the source drivers (*204*) via a single path.

Figure 3 illustrates the source drivers (*204*) and the gate drivers (*202*) having a common or shared coupling to the DC/DC converter (*130*).

In contrast, Figure 5 illustrates the source drivers (*204*) and the gate drivers (*202*) having two distinct and independent couplings to the power supply (*258*).

Figure 5 illustrates an input interface coupled only to a timing sequence control unit (*256*).

In contrast, Figure 3 illustrates no "input interface" whatsoever.

Figure 5 illustrates what appear to be multi-bit outputs from the source drivers (*204*) and the gate drivers (*202*) to the panel (*250*).

In contrast, Figure 3 illustrates no multi-bit outputs whatsoever.

The traversal is on the ground(s): "*Next, pertaining to Sub-Species A to E, the timing-sequence control units shown in different figures are very similar but have different names or are illustrated in varying degrees of detail. For example, as indicated in paragraphs [0038], [0039] and [0040], the timing-sequence control units shown in FIGs. 8 and 9 are equal, wherein the control block 256b comprises the processing unit 402 and the storage device 400. Hence, the fourth embodiment and the fifth embodiment do not illustrate different timing-sequence control units, instead, the fifth embodiment only illustrates the timing-sequence control unit in further detail.*" (see Page 8 of the *22 January 2009* Election). This is not found persuasive.

There is an examination and search burden for argued ***Sub-Species D and E*** due to the following mutually exclusive characteristics:

Specification Paragraph 39 states, "*The above [FIG. 8] control block 256b as shown in FIG. 9* ***can include*** *the processing unit 402 and the storage device 400.*"

Clearly, the verb "***can include***" infers the disclosure of two species here:

1. The control block 256b including the processing unit 402 and the storage device 400.

2. The control block 256b not including the processing unit 402 and the storage device 400.

The traversal is on the ground(s): "*Similarly, pertaining to Sub-Sub-Species I and II, the first embodiment and the second embodiment do not illustrate different programmable interfaces, instead, the second embodiment only illustrates the programmable interface in further detail.*" (see Page 8 of the *22 January 2009* Election). This is not found persuasive.

There is an examination and search burden for argued ***Sub-Sub-Species 1 and 2*** due to the following mutually exclusive characteristics:

Figure 7 illustrates a shift register and a line latch coupled between a decoder and a plurality of DACs.

In contrast, Figure 6 illustrates no "shift register," no "line latch," and no plurality of DACs. The decoder (*304*) is directly coupled to a single DAC (*306*).

The Applicant also argues, "*Furthermore, Applicant also respectfully submits that although the color management interface system disclosed in the specification is divided into two parts, the present application discloses only a single invention instead of two inventions, since the components therein function in cooperation for a single purpose.* ***Applicant respectfully***

asserts that a single invention should not be viewed as two merely because the components therein are spatially separated." (see Pages 8-9 of the *22 January 2009* Election).

However, seemingly contradicting the above logic, in the 14 May 2008 response, the Applicant argues, "*the* ***clock generation circuit 1008 in FIG. 9*** *of Naito is not included in the* ***signal-processing circuit 200 in FIG. 2*** *of Naito. In other words, the signal-processing circuit 200 of Naito does not output clock signals. Hence,* ***the signal-processing unit 200 of Naito is clearly distinct from the timing sequence control unit*** *of the instant case.*" (see Page 14 of the *14 May 2008* Amendment).

The requirement is still deemed proper and is therefore made FINAL.

4. ***Claims 5, 9, 10, 15-18, and 20 are withdrawn*** from further consideration pursuant to 37 CFR 1.142(b), as being drawn to nonelected species, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on *22 January 2009*.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-4, 6-8, 11-14, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Kang et al (US 2002/0063666 A1)*** in view of the instant ***Application's Admitted Prior Art (AAPA)***.

Regarding claim 1, ***Kang*** discloses a color management structure [*Fig. 14*] for a panel display [*Fig. 14: 145*], comprising:

a display array unit [*Fig. 14: Clc*];

a plurality of gate drivers [*Fig. 14: 144*];

a plurality of source drivers [*Fig. 14: 143*],

said plurality of gate drivers and said plurality of source drivers driving said display array unit to display an image [*Fig. 14: video data*]; and

a timing sequence control unit [*Figs. 14 & 15: 142*],

said timing sequence control unit outputting a plurality of signals [*Figs. 14 & 15: Gsp, Dclk, RGB, γ data, clock*] to said plurality of gate drivers and said plurality of source drivers to drive said display array unit,

said timing sequence control unit outputting a clock signal [*Figs. 14 & 15: clock*] and

a digital color management data [*Figs. 14 & 15: γ data, aka User Selectable Gamma Modes A to D -- see also Fig. 9: I^2C Data*] to said plurality of source drivers (*see the entire document, including Paragraphs 69-74*).

Should it be shown that ***Kang*** discloses the claimed subject matter of "*gate/source drivers*" with insufficient specificity:

The ***AAPA*** discloses a color management structure [*Fig. 2*] for a panel display [*Fig. 2: 120*], comprising:

a display array unit [*Fig. 2: pixel array*];

a plurality of gate drivers [*Fig. 2: 124*];

a plurality of source drivers [*Fig. 2: 122*],

said plurality of gate drivers and said plurality of source drivers driving said display array unit to display an image; and

a timing sequence control unit [*Fig. 2: 126*],

said timing sequence control unit outputting a plurality of signals [*Fig. 2: clock & color data from 126 to 122 & 124*] to said plurality of gate drivers and said plurality of source drivers to drive said display array unit,

said timing sequence control unit outputting a clock signal [*Fig. 2: clock*] and

a digital color management data [*Fig. 2: color data*] to said plurality of source drivers (*see the entire **AAPA**, including Paragraphs 7-10*).

Kang and the ***AAPA*** are analogous art, because they are from the shared inventive field of driving, timing control, and gamma correction of liquid crystal displays.

Therefore, it would have been obvious to use the ***AAPA's*** gate/source drivers in the place of ***Kang's*** gate/source drivers, because the substitution of one known arrangement of gate/source drivers for another would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

See KSR International Co. v. Teleflex Inc., et al., Docket No. 04-1350 (U.S. 30 April 2007).

Regarding claim 2, ***Kang*** discloses said digital color management data is adjustable [*Fig. 9: via 100*] (*see the entire document, including Paragraphs 48-61 -- wherein the Gamma Modes A to D are selectable/adjustable via the user interface*).

Regarding claim 3, ***Kang*** discloses said panel display is a liquid crystal display (*see the entire document, including Paragraph 69*).

Regarding claim 4, this claim is rejected by the reasoning applied in rejecting claim 2; furthermore, ***Kang*** discloses said timing sequence control unit includes:

a timing controller [*Fig. 9: 91*] receiving a system input [*Fig. 9: from 100*] and providing said clock signal [*Fig. 9: I^2C Clock*]; and

a color management control block [*Fig. 9: 91*], coupled to said timing controller, outputting said digital color management data and said clock signal to said plurality of source drivers [*Fig. 8: 83; Fig. 9: 96-99; Fig. 14: 143; Fig. 15: 154-156*] (*see the entire document, including Paragraphs 48-61*).

Regarding claim 6, ***Kang*** discloses each of said plurality of source drivers includes:

a source drive circuit [*Fig. 9: 97; Fig. 15: 156*] to drive said display array unit; and

a programmable data interface [*Fig. 9: 92, 93; Fig. 15: memory within 142, 152*] receiving said digital color management data [*Fig. 9: I^2C Data; Fig. 15: γ data*] and said clock signal [*Fig. 9: I^2C Clock; Fig. 15: Clock*] to parallel output a plurality of color voltage level signals [*Figs. 9, 10: GMA*] to said source drive circuit (*see the entire document, including Paragraphs 48-61*).

Regarding claim 7, ***Kang*** discloses said plurality of color voltage level signals includes a plurality of color gamma voltage level data (*see the entire document, including Paragraphs 48-61 -- for red, green, and blue video data*).

Regarding claim 8, ***Kang*** discloses said programmable data interface includes:

an input interface [*Fig. 9: 92*] receiving said digital color management data [*Fig. 9: I^2C Data*] and said clock signal [*Fig. 9: I^2C Clock*] and translating said digital color management data [*Fig. 9: 6-bit serial gamma data*] via a data format;

a decoder [*Fig. 10: 101*] receiving said translated digital color management data and said clock signal and decoding said translated digital color management data, and outputting a decoded data [*Fig. 11: D5-D0*] and a control signal [*Fig. 11: A3-A0, SD-SA*]; and

a digital-to-analog converting unit [*Fig. 10: 103*] receiving said decoded data, said control signal, and said clock signal, and parallel outputting said plurality of color voltage level signals (*see the entire document, including Paragraphs 48-61 -- for red, green, and blue video data*).

The ***AAPA*** additionally discloses a digital-to-analog converting unit [*Fig. 1: 106*] receiving decoded data [*Fig. 1: VGMA1-VGMA14*], a control signal [*Fig. 1: POL*], and a clock signal [*Fig. 1: CLK1*], and parallel outputting a plurality of color voltage level signals [*Fig. 1: Y1-Y384*] (*see the entire **AAPA**, including Paragraphs 7-10*).

Regarding claim 11, ***Kang*** discloses said timing sequence control unit is integrated into an application specified integrated circuit (*see the entire document, including Paragraph 70*).

The ***AAPA*** additionally discloses said timing sequence control unit is integrated into an application specified integrated circuit [*Fig. 2: ASIC*] (*see the entire **AAPA**, including Paragraphs 7-10*).

Regarding claim 12, this claim is rejected by the reasoning applied in rejecting claim 6.

Regarding claim 13, this claim is rejected by the reasoning applied in rejecting claim 7.

Regarding claim 14, this claim is rejected by the reasoning applied in rejecting claim 8.

Regarding claim 19, this claim is rejected by the reasoning applied in rejecting claim 1.

Response to Arguments

7. Applicant's arguments filed *14 May 2008* have been fully considered but they are not persuasive.

Applicant's arguments with respect to *claims 1-4, 6-8, 11-14, and 19* have been considered but are moot in view of the new ground(s) of rejection.

By such reasoning, rejection of the claims is deemed necessary, proper, and thereby maintained at this time.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The documents listed on the attached '*Notice of References Cited*' are cited to further evidence the state of the art pertaining to color management structures.

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (571) 272-7678. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen can be reached on (571) 272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jeff Piziali/
Primary Examiner, Art Unit 2629
3 May 2009